REMARKS

In response to the Office Action, claims 1, 19 and 21 have been amended and claims 7 and 22 have been canceled. New claims 42-45 have been submitted for the Examiner's consideration. Accordingly, claims 1-6, 8-21 and 23-45 are currently pending while claims 4-6, 10-18, 20 and 25-33 have been withdrawn.

Support for amendments to claim 1 (which incorporates the subject matter of claim 7) can be found, for example, on page 22, lines 13-19, support for amendments to claim 19 can be found, for example, on page 52, lines 8-17, and support of amendments to claim 21 (which incorporates the subject matter of claim 22) can be found for example, on page 14, lines 3-5. Support for new claim 42 can be found on, for example, page 26, lines 21-24, support for new claim 43 can be found on, for example, page 27, lines 6-8, support for new claim 44 can be found on, for example, page 27, lines 8-9 and support for new claim 45 can be found on, for example, page 29, lines 15-19.

Claims 1-3, 7, 8, 21-23, 34, 35 and 37-41 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,242,348 to Kamal et al. (hereinafter Kamal).

Amended claim 1 recites a method for manufacturing a semiconductor device including a member which is partially silicified, comprising the steps of a) performing a first thermal annealing to form a polycrystalline first silicide film that is rich in metal on the semiconductor layer, b) implanting impurity ions into the first silicide film so as to change the first silicide film into an amorphous second silicide film, c) performing second thermal annealing to change the amorphous second silicide film into a polycrystalline third silicide film, and d) in the step of implanting the impurity ions, implanting the impurity ions into a surface portion of the semiconductor layer under the second silicide film, so as to change the surface portion of the semiconductor layer into an amorphous state and to a depth at which the third silicide film will be formed through the second thermal annealing in the step (e). In other words, the amorphous semiconductor layer, by the implantation of the impurity ions, is converted into the third silicide film. Any damage or defect caused by tuning the semiconductor layer into an amorphous state is in the third silicide film, not in the semiconductor layer, and as a result, abnormal junction leaks can be suppressed.

According to the present invention, in the formation of a third silicide film, disruptions or substantial surface irregularities in the silicide film due to silicide film agglomeration can be suppressed, so as to more effectively reduce resistance. Moreover,

since crystal grains of the third silicide film grow uniformly, spiking is less likely to occur, and abnormal junction leaks can thereby be suppressed.

In contrast, the Kamal patent discloses a semiconductor device that is formed by: a) performing a first thermal annealing to form cobalt silicide (CoSi) layers 122 and 124, b) implanting boron and nitrogen into a substrate on which the cobalt silicide (CoSi) layers 122 and 124 are formed, and c) subsequently, performing a second thermal annealing to form cobalt silicide ($CoSi_2$) layers 132 and 134.

While Kamal discloses boron implantation and nitrogen implantation into a substrate on which the cobalt silicide (CoSi) layers 122 and 124 are formed, Kamal fails to disclose at what depth the cobalt silicide layers turn into an amorphous state. Thus, Applicant respectfully submits that Kamal does not disclose or suggest implanting the impurity ions into a surface portion of the semiconductor layer under the second silicide film, so as to change the surface portion of the semiconductor layer into an amorphous state and <u>to a depth at which the third silicide film will be formed through the second thermal annealing in the step (e)</u>, as now recited in independent claim 1.

Also, in Kamal, the boron dopant implantation generates carriers in order to reduce resistances of a bilayer CoSi/Si stack structure 126, which forms a gate electrode, and a silicon substrate 102, which forms source/drain regions. Kamal, however, does not disclose implanting the impurity ions into a surface portion of the semiconductor layer under the second silicide film, <u>so as to change the surface portion of the semiconductor layer into an amorphous state</u>, now recited in independent claim 1.

Moreover, Applicant submits that Kamal teaches away from the features of the presently claimed invention. A depth of the amorphous layer in Kamal appears to be much deeper than a depth at which the $CoSi_2$ layer will be formed through the second thermal annealing. If the layer turns into an amorphous state only to a depth at which a $CoSi_2$ layer will be formed through the second thermal annealing, almost all boron is injected to the $CoSI_2$ layer, and, as a result, the reduced resistance of the silicon layer under the $CoSI_2$ layer cannot be realized. As illustrated in Fig. 9 of Kamal, a high concentration region (1E+19) in impurity distribution of nitrogen is formed near an interface with the gate insulating film, as compared with the impurity distribution of cobalt. Accordingly, Applicants submit that a depth of the amorphous layer in Kamal is much deeper than a depth at which a $CoSi_2$ layer will be formed through the second thermal annealing, as with the present invention.

Amended claim 21 recites a method for manufacturing a semiconductor device including a member which is partially silicified, comprising the steps of a) forming a metal film on a semiconductor layer of a substrate, b) performing first thermal annealing to cause a silification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first silicide film that is rich in metal on the semiconductor layer, c) removing an unreacted portion of the metal film after the step (b), d) introducing nitrogen into the semiconductor layer in a step after the step (a) and before the step (c), e) after the step (d), performing second thermal annealing to change the first silicide film into a second silicide film, the second silicide film being at least a part of the member, f) wherein in the step (d), the nitrogen is introduced so that a nitrogen concentration in the semiconductor layer is 10^{17} cm^{-3} or less after the step (e). Thus, in accordance with the present invention, after the formation of the second silicide film, the nitrogen is introduced so that a nitrogen concentration in the semiconductor layer is 10^{17} cm^{-3} or less.

On the other hand, in Kamal, nitrogen ions are implanted so that a nitrogen peak concentration is located in the silicon layer, which is deeper than the CoSi/silicon interface. As illustrated in Fig. 9 of Kamal, a high concentration region (1E+19) in impurity distribution of nitrogen is formed near an interface with the gate insulating film, as compared with the impurity distribution of cobalt. In other words, the nitrogen concentration in the semiconductor layer, after the formation of a $CoSi_2$ layer through the second thermal annealing, is set at a much higher concentration than 10^{17} cm^{-3}, set forth in the presently claimed invention. Thus, Applicants submit that Kamal does not teach or suggest that nitrogen is introduced so that a <u>nitrogen concentration in the semiconductor layer is 10^{17} cm^{-3} or less after the step (e)</u>, as now set forth in independent claim 21. Accordingly, as set forth above, Kamal does not disclose or suggest the claimed subject matter and Applicant respectfully requests reconsideration and withdrawal of the rejections and submits that claims 1-3, 7-8, 21-23 34, 35 and 37-41 are allowable over Kamal.

On page 4 of the Office Action, claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kamal in view of U.S. Patent No. 5,659,194 to Iwamatsu et al.

Applicant submits that Iwamatsu fails to cure the deficiencies of Kamal and submits that claim 9 is allowable for at least the reasons discussed with respect to independent claim 1, as well as for reasons of its own.

Also on page 4 of the Office Action, claim 24 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kamal and further in view of U.S. Patent No. 5,627,105 to Delfino et al. and U.S. Patent No. 4,701,349 to Koyanagi et al.

Applicants respectfully submit that neither Delfino nor Koyanagi solve the deficiencies of Kamal. Further, Applicant submits that Iwamatsu also fails to cure the deficiencies of Kamal and submits that claim 24 is allowable for at least the reasons discussed with respect to independent claim 21, as well as for reasons of its own.

On page 4 of the Office Action, claims 19 and 36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kamal in view of U.S. Patent No. 5,659,194 to Frenkel et al.

Amended claim 19 recites a method for manufacturing a semiconductor device including a) forming a metal film whose main component is cobalt on a semiconductor layer of a substrate, b) performing first thermal annealing to cause a silicification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first cobalt silicide film that is rich in cobalt on the semiconductor layer, c) removing an unreacted portion of the metal film; and d) performing second thermal annealing at a temperature higher than a temperature of the first thermal annealing, and at a temperature of 725 °C or less in which no $CoSi_2$ crystal gains occurs, to change the first cobalt silicide film into a second cobalt silicide film, the second cobalt silicide film being at least a part of the member. In the present invention, the second thermal annealing to form the second cobalt silicide film is performed at a higher temperature than that of the first thermal annealing, and at a temperature of 725 °C or less in which no $CoSi_2$ crystal gains occurs.

On the other hand, in Kamal, the second thermal annealing is performed at a temperature of 800-950 °C to form the $CoSi_2$ layer. Thus, the present invention is distinguished from Kamal in view of a temperature of the heat annealing and the silicide structure. Turning to Frenkel, used to solve the deficiencies of Kamal, the second heat annealing is performed at a temperature of 700-900 °C to form a $CoSi_2$ layer.

However, Applicant respectfully submits that even if Frenkel is considered to solve the deficiencies of Kamal, it cannot be combined with Kamal to teach the presently claimed invention since Frenkel, itself actually teaches away from the presently claimed invention. For example, Frenkel performs a second heat annealing at a temperature of 700-900 °C to form a $CoSi_2$ layer. However, since Frenkel performs a second heat annealing at a temperature of 700-900 °C, any combination with Kamal would not take into account

performing second thermal annealing at a temperature higher than a temperature of the first thermal annealing, and at a temperature of 725 °C or less in which no $CoSi_2$ crystal gains occurs. As discussed on page of the present specification, the second rapid thermal annealing is performed at a temperature of 725 °C or less in which no $CoSi_2$ crystal gains occurs. Frenkel however does not appear to need or want the result obtained by the present invention. Accordingly, Applicants respectfully submit that Frenkel teaches away from the claims and objects of this embodiment of the present invention. As none of the cited prior art, either alone or in combination, discloses or suggests the claimed subject matter, claims 19 is allowable.

Applicant submits that claim 34 is allowable for at least the reasons discussed with respect to independent claim 19, as well as for reasons of its own.

Given the above, none of the cited prior art discloses or suggests the claimed subject matter. Therefore, Applicant's respectfully submit that the application is now in condition for allowance. A prompt passage to issuance is therefore earnestly solicited.

Respectfully submitted,

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